

CLAIM AMENDMENTS

Please amend claims 32, 39 and 43, all without prejudice, as indicated on the following listing of all the claims in the present application after this Amendment:

1.-31. (cancelled)

32. (amended) A non-volatile memory, comprising:

an array of memory storage units;

a controller;

a plurality of sense amplifiers for sensing a group of memory storage units in parallel;
each of said plurality of sense amplifiers having properties dependent on operating environment and a set of control signals; and

a reference circuit having elements with properties representative of said plurality of sense amplifiers and sharing a common operating environment with said plurality of sense amplifiers, said reference circuit, responsive to said elements operating in the operating environment, generating said set of control signals such that said plurality of sense amplifiers are controlled to have its properties substantially insensitive to the operating environment[.] and

each sense amplifier further comprising:

a discriminator coupled to receive a conduction current of an associated memory cell, said discriminator discriminating whether the conduction current is higher or lower than a predetermined demarcation current value;

a latch being set to register the associated memory cell in response to said discriminator identifying a conduction current higher than said predetermined demarcation current value;

an inhibitor to turn off the conduction current of the associated memory cell;

an inhibitor enabler responsive to said plurality of sense amplifiers having their discriminators completed their identifications and said latch being set; and wherein

said controller controls said plurality of sense amplifiers to operate a predetermined number of times before reading out the determined memory state.

33. (previously presented) The non-volatile memory of claim 32, wherein said properties include a threshold voltage of a component transistor.

34. (previously presented) The non-volatile memory of claim 32, wherein said properties include a capacitance of a component capacitor.

35. (previously presented) The non-volatile memory of claim 32, wherein said operating environment includes a given power supply.

36. (previously presented) The non-volatile memory of claim 32, wherein said operating environment includes a given temperature.

37. (previously presented) The non-volatile memory of claim 32, wherein said set of control signals includes a timing signal calibrated to a reference current.

38. (previously presented) The non-volatile memory of claim 32, wherein said set of control signals includes a voltage for controlling a voltage clamp.

39. (amended) A non-volatile memory, comprising:
a plurality of sense amplifiers for sensing a group of memory storage units in parallel,
each of said plurality of sense amplifiers having properties dependent on operating environment
and a set of control signals;

a controller;

a reference circuit having elements with properties representative of a typical member of
said plurality of sense amplifiers and located in a common operating environment with said
plurality of sense amplifiers; and

means for generating said set of control signals, responsive to said elements operating in
the operating environment such that said plurality of sense amplifiers is controlled to have its
properties substantially insensitive to the operating environment[.] and

each sense amplifier further comprising:

a discriminator coupled to receive a conduction current of an associated memory cell, said discriminator discriminating whether the conduction current is higher or lower than a predetermined demarcation current value;

a latch being set to register the associated memory cell in response to said discriminator identifying a conduction current higher than said predetermined demarcation current value;

an inhibitor to turn off the conduction current of the associated memory cell;

an inhibitor enabler responsive to said plurality of sense amplifiers having their discriminators completed their identifications and said latch being set; and wherein

said controller controls said plurality of sense amplifiers to operate a predetermined number of times before reading out the determined memory state.

40. (previously amended) The non-volatile memory as in any one of claims 32-39, wherein:

said plurality of memory storage units are flash EEPROM.

41. (previously amended) The non-volatile memory as in any one of claims 32-39, wherein:

each memory storage unit stores one bit of data.

42. (previously presented) The non-volatile memory as in any one of claims 32-39, wherein:

each memory storage unit stores more than one bit of data.

43. (amended) A method of controlling a plurality of sensing circuits for a non-volatile memory, comprising:

(a) providing a predetermined demarcation current value to discriminate between two memory states;

(b) sensing the plurality of memory cells in parallel;

(c) sensing to identify those memory cells having conduction currents higher than said predetermined demarcation current value;

(d) inhibiting the conduction currents of those higher current memory cells after identifying all those higher current memory cells among said plurality of memory cells being sensed in parallel;

(e) repeating (b) to (d) for a predetermined number of times; and

(f) sensing the plurality of memory cells in parallel in a final pass; and
wherein said sensing in (b), (c) and (f) further comprises:

providing a plurality of sense amplifiers for sensing a group of memory storage units in parallel, each of said plurality of sense amplifiers having properties dependent on operating environment and a set of control signals;

locating a reference circuit having elements with properties representative of a typical member of said plurality of sense amplifiers in a common operating environment with said plurality of sense amplifiers; and

generating said set of control signals, responsive to said elements operating in the operating environment such that said plurality of sense amplifiers is controlled to have its properties substantially insensitive to the operating environment.

44. (previously presented) The method as in claim 43, wherein:
said plurality of memory storage units is flash EEPROM.

45. (previously presented) The method as in claim 43, wherein:
each memory storage unit one bit of data.

46. (previously presented) The method as in claim 43, wherein:
each memory storage unit stores more than one bit of data.